High-Speed Information Processing for Laser-locking System Applied to Optomechanical Cavities

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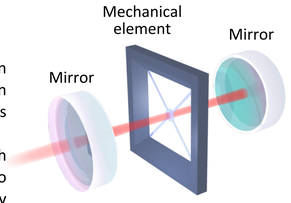
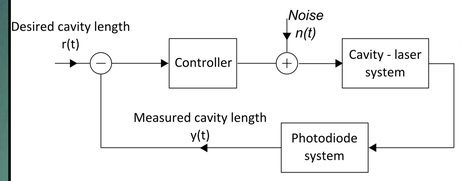
Introduction

Optomechanics is concerned with the interaction between light and mechanical elements. The interaction is maximum when the power circulating in the cavity is maximum.
Power is maximum when the laser is in resonance with the cavity length. The objective of this project is to cancel the effect of the mechanical noise on the cavity length.



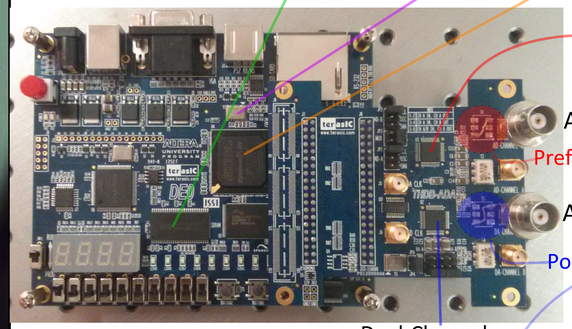


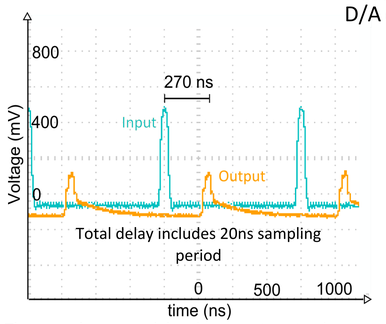
- The desired cavity length is set by the user (via signal r(t));
- The controller uses piezoelectric elements in the cavity-laser system to adjust the cavity length, with mechanical noise n(t);
- The photodiode system outputs a measurement of the cavity length y(t);
- The controller compares the difference between the measured and desired cavity length and acts accordingly;

The first part of the project focuses on designing signal processing hardware capable of acting as an arbitrary filter. Filter design is part of future development. The processing hardware must:
- work at high speed (sampling >> 100 kHz);
- be easily adaptable to various experimental setups.

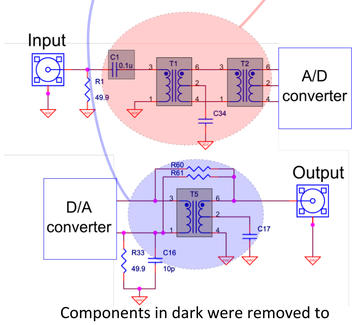
We chose to base the project on FPGA-based hardware because of its speed advantage over CPU-based hardware.

Setup



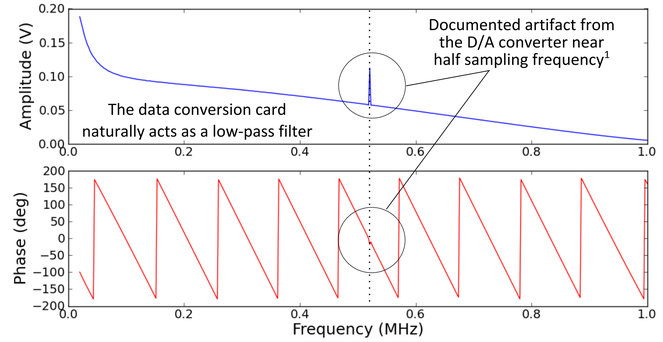


The setup's group delay (or reaction time) was determined to be around 250 ns for all frequencies.



Components in dark were removed to allow for low frequencies (< 100kHz)

Setup (continued)



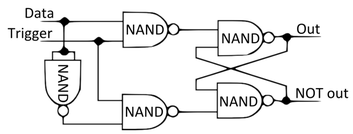
Implementation

Given a transfer function in the Laplace s-domain, it is straightforward to translate it in discrete-time hardware[2]. This translation results in a relation between the previous and current inputs and previous ouputs. Thus, implementing a filter results in implementing a relation of the form:

$$y[n] = a_0 x[n] + a_1 x[n-1] + a_2 x[n-2] + \dots + b_1 y[n-1] + b_2 y[n-2] + \dots$$

Memory

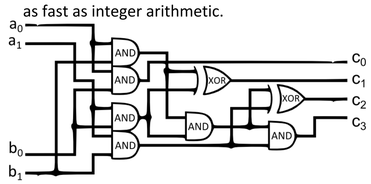
Registers (figure below) were wired in parallel to form a custom Random Access Memory (RAM).



This custom memory increases reaction time by ~350ns for a typical 8-term difference equation, compared to RAM.

Arithmetic

The setup uses fixed-point arithmetic, which is as fast as integer arithmetic.

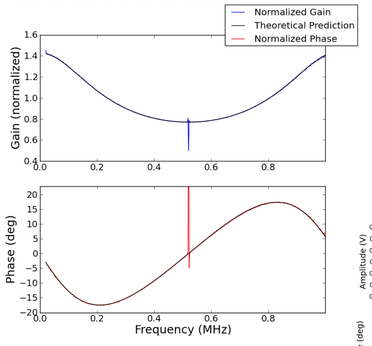


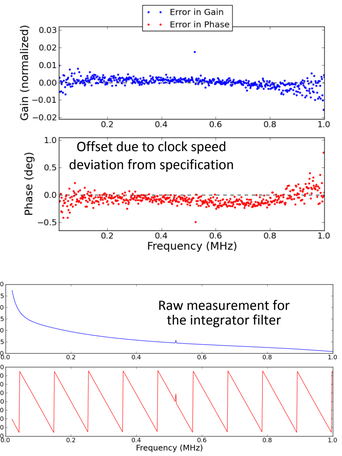
Integer binary multipliers (figure above) were wired and provide near-instant multiplication (< 20ns).

Testing

All results presented are normalized to the intrinsic transfer function. Sampling frequency was set to 1MHz for all tested filters.

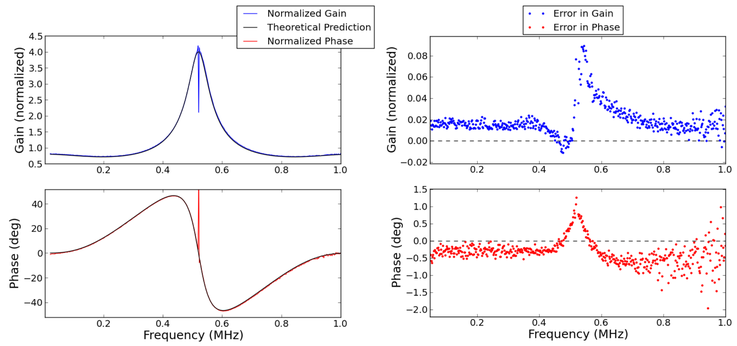
Integrator filter



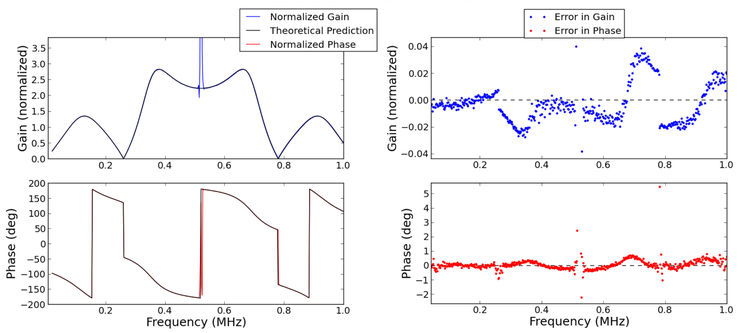


Testing (continued)

Resonance filter



Double Peak filter



Conclusion

We created a system that is predictable and easily customizable. We were able to reduce the setup's reaction time close to the hardware limitations by using a custom type of memory and by approximating real-number arithmetic with fixed-point arithmetic. In the future:
- We may create our own data conversion card. This would enable us to control every parameter: resolution, dynamic range, maximum sampling frequency, and group delay;
- We are currently looking in approximating an inverse to the intrinsic transfer function;
- We still have to design the transfer function that can realize the feedback-loop presented in the Introduction.

References

[1] Analog Devices, *http://goo.gl/hFG5j5*. Manufacturer datasheet, 2011.
[2] Oppenheim et al., *Discrete-time Signal Processing*. Prentice-Hall, New Jersey, second edition, 1999.
Poster background provided by Wallpaper Beautiful at goo.gl/txM6oC

Acknowledgments

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